Single Event Upset Characterization of Microsemi RISC-V Softcore CPUs on Polarfire MPF300T-1FCG1152E Field Programmable Gate Arrays Using Proton Irradiation

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***Abstract*—SEU cross-sections of the Polarfire FPGA programmed with various Microsemi RISC-V Softcore CPUs are presented. Upset rates in the space radiation environment are estimated and found to be acceptable for low orbit missions.**

***Keywords*— Single event upset; Proton irradiation; RISC-V; Polarfire; FPGA**

I. INTRODUCTION

In this paper, the approach followed to characterize the dynamic single event upset (SEU) susceptibility of Microsemi RISC-V softcore CPU variants on the Polarfire MPF300T-1FCG1152E are presented. The experimental test setups, test results obtained, and analysis of these results, are described. Based on the test results obtained and using the Figure of Merit (FOM) technique [1], SEU rates are determined for a typical low earth orbit mission. Single event latchup (SEL) and total dose effects are discussed.

Observed upsets are categorized as either Trap, CPU Halt or Unreadable. Trap indicates that an internal software interrupt occurred while CPU Halt indicates that the terminal ceased receiving new data from the board and the LEDs indicators showed that the CPU had ceased operation. Unreadable indicates that the terminal ceased to receive readable messages. All configurations were tested for a similar time interval and were shown to operate without errors without exposure to proton irradiation before and after irradiation.

The RISC-V softcore CPUs are based on the Rocket-Chip 32-bit opensource core and are designed to work with Microsemi's Polarfire TG4 and IGLOO2 FPGAs. The softcore CPUs possess 8 kbyte integrated instruction and data caches and industry standard JTAG debug interfaces. SEU testing and analyses are undertaken to evaluate the performance of the Polarfire MPF300T-1FCG1152E FPGA programmed with the Microsemi RISC-V softcore CPUs in the space radiation environment.

For this test proton irradiation was performed at the Tri-University Meson Facility (TRIUMF) Proton Irradiation Facility (PIF), located on the campus of the University of British Columbia (UBC), British Columbia, Canada. Beamline 2C of the PIF was used for characterization of the RISC-V softcore CPUs using 105 MeV protons [2]. The outcome of this research was the single event effects (SEE) characterization of Microsemi RISC-V softcore CPU variants on the Polarfire MPF300T-1FCG1152E.

II. DEVICES UNDER TEST OVERVIEW

The RISC-V softcore CPUs tested were the, MIV_RV32IMAF_L1_AHB, MIV_RV32IMA_L1_AHB, and MIV_RV32IMA_L1_AXI. These CPUs utilise 26 000, 10 000 and 10 000 logic elements, respectively. The Polarfire FPGA used in testing the CPUs was the MPF300T-1FCG1152E, which is fabricated from a 28 nm non-volatile process technology and operates with a core voltage of 1.05 V. Additional information can be found on the manufacturer's data sheet [3] and the product webpage [4].

III. TESTING METHODOLOGY, SETUP, AND PROCEDURE

A. *Test Approach*

The MPF300T-1FCG1152E was configured in three ways for this characterization. One configuration loaded the MIV_RV32IMAF_L1_AHB another the MIV_RV32IMA_L1_AHB and the third MIV_RV32IMA_L1_AXI. Each of these softcore CPUs were programmed with a matrix multiplication algorithm which randomly generated matrices and transmitted results as well as time stamps via UART connection to a nearby laptop. When programming the MIV_RV32IMAF_L1_AHB floating point values were generated for the matrices instead of integers which were used for the other two softcore CPUs.

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B. *SEU Test Setup*

The setup consisted of the MPF300-VIDEO-KIT-NS evaluation board (EB) with FPGA, local laptop, camera, ethernet switch, power supply and remote laptop. Power was controlled remotely by the GPIB capable Power supply. Current probe monitored the EB supply input for any current spikes and anomalies. The FPGA was connected to a local laptop via a UART connection so that the board could be remotely re-programmed as well as observe results. A camera was also used to remotely observe the LEDs to help determine the softcore CPUs operational state. Both the camera and the local laptop were remotely controlled via ethernet using a secondary remote laptop. A diagram of the test setup is shown in Fig. 1.

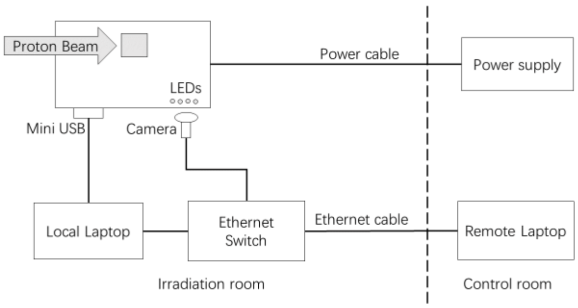

Figure 1. SEU Test Setup

C. *SEU Test Procedures*

For every run of tests, the MPF300T-1FCG1152E was programmed with the corresponding configuration of RISC-V softcore CPU and algorithm. Once the executing the proton beam was applied to the DUT. In the event that a SEU was detect the beam was halted and the fluence to upset, upset signature and recovery method were recorded. In addition to this the EB power rail was monitored.

D. *Test Facility*

Testing was performed at the TRIUMF PIF located on the UBC campus. This general purpose proton irradiation facility consists of two beam lines located in the same room. Beam line 1B provides protons with energies ranging from 180 to 520 MeV. Beam line 2C provides proton energies up to 120 MeV. Beam line 2C is also used for proton therapy. The beam line characteristics are described in Table I [2]. Beam line 2C was used in this test campaign.

TABLE I
TRIUMF Proton Irradiation Facility Specification [2]

	Beam Line 1B	Beam Line 2C
Energy (MeV)	180-520 120-180 by degrader	65-120 20-65 by degrader
Intensity (protons/cm^2/s)	10^5 - $4x10^7$	10^5 - 10^8
Field Size Square (cm^2)	4 - 225	1 - 49

IV. TEST OBJECTIVES AND RESULTS

A. *Objectives*

The objectives of these tests were: (1) Determine the upset cross section for different variants of the Microsemi RISC-V softcore CPU loaded on the MPF300-VIDEO-KIT-NS, (2) Investigate possible latch up sensitivity, (3) Establish the total dose performance.

B. *Results*

The RISC-V softcore CPU SEU test results for the matrix multiplication algorithm are show in Tables II, III and IV. The display the data for the RV32IMAF_AHB, RV32IMA_AHB and RV32IMA_AXI cores. The recorded data consists of fluence to upset, upset signature and recovery method.

TABLE II
Mi-V_RV32IMAF_AHB

Fluence to Upset (p/cm^2)	Upset Signature	Recovery Method
6.91E+09	Trap	Power cycle
2.46E+09	Trap	Power cycle
1.47E+09	Trap	Power cycle
3.35E+09	Trap	Power cycle
5.98E+08	CPU Halt	Power cycle
2.10E+08	Unreadable	Power cycle
4.90E+08	Trap	Power cycle
2.99E+08	Trap	Power cycle
1.20E+09	Trap	Power cycle
1.65E+09	Trap	Power cycle

TABLE III
Mi-V_RV32IMA_AHB

Fluence to Upset (p/cm^2)	Upset Signature	Recovery Method
1.98E+09	Unreadable	Power cycle
2.45E+09	Unreadable	Power cycle
2.42E+09	Trap	Power cycle
1.56E+09	Unreadable	Power cycle
6.70E+08	Trap	Power cycle
9.18E+08	CPU Halt	Power cycle
8.15E+09	Trap	Power cycle
1.24E+09	Trap	Power cycle
2.12E+09	Trap	Power cycle
1.98E+08	Trap	Power cycle

TABLE IV
Mi-V_RV32IMA_AXI

Fluence to Upset (p/cm^2)	Upset Signature	Recovery Method
6.31E+09	CPU Halt	Power cycle
7.71E+08	CPU Halt	Power cycle
3.85E+08	Unreadable	Power cycle
1.02E+09	Trap	Power cycle
6.80E+08	Trap	Power cycle
8.68E+09	Trap	Power cycle
1.09E+09	CPU Halt	Power cycle
1.28E+09	Unreadable	Power cycle
3.34E+09	Trap	Power cycle
3.83E+08	CPU Halt	Power cycle

V. ANALYSIS AND DISCUSION

A. *SEU Cross-sections*

The proton SEU cross-section of the MIV_RV32IMAF_L1_AHB, MIV_RV32IMA_L1_AHB, and MIV_RV32IMA_L1_AXI RISC-V softcore CPUs are $5.37x10^{-10}$ cm^2/processor, $4.61x10^{-10}$ cm^2/processor, and $4.17x10^{-10}$ cm^2/processor, respectively. The SEU cross-section is somewhat dependent on the RISC-V softcore CPU FPGA resource utilization.

B. *Single Event Latchup*

No SEL or current spikes on the FPGA power rail due to protons were observed. Advanced micro-circuits have shown SEL to protons [5]. Devices susceptible to proton SEL are considered unacceptable for space missions. The MPF300T-1FCG1152E was irradiated with the equivalent of at least 12.52 years heavy ion fluence up to a LET of approximately 10 $MeVcm^2/mg$ [6], with no SEL observed. Based on this work and that of O'Neill et al., this suggests the probability of heavy ion SEL is low if these devices were used on the Space Station or any other low earth orbit short duration mission [7].

C. *Total Dose*

The MPF300T-1FCG1152E received a total fluence of $64.3x10^9$ p/cm^2 at 105 MeV, equivalent to a total dose of 5.7 krad (Si). No change in post irradiation FPGA power supply current was observed. This total dose tolerance is suitable for many low earth orbit missions. The total dose tolerance of this device is anticipated to be considerably higher.

D. *Single Event Upset Rate*

Using the FOM [1] technique on the Space Station, assuming 0.2" Al shielding, in a space station orbit (51.6°, 420 km circular), the upset rate for the MPF300T-1FCG1152E is estimated to be (protons and heavy ions) for MIV_RV32IMAF_L1_AHB, MIV_RV32IMA_L1_AHB, and MIV_RV32IMA_L1_AXI configurations 0.000739/day, 0.000635/day, and 0.000575/day, respectively. This device with the appropriate mitigation scheme could be used on many low earth orbit short duration missions.

VI. CONCLUSIONS

The Microsemi RISC-V softcore CPUs in combination with the MPF300T-1FCG1152E Polarfire FPGA provide considerable advantages over SRAM FPGA and ASIC configurations. It's SEE and total dose are acceptable for low earth orbit, short duration missions.

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